

# Qseven™ Specification Revision 1.1

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***Qseven™ pinout, electromechanical description and implementation guidelines***

***Qseven™ Specification***

***Revision 1.1***

# Qseven™ Specification Revision 1.1

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## Revision History

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Revision	Date (dd.mm.yy)	Author	Revision History
1.0	01.07.08	Qseven™ Consortium	Official Release
1.1	04.08.08	Qseven™ Consortium	Corrected overall height dimension in Figure 1-1 Overall Height including Heatspreader of the Qseven™ Module. Changed pin assignment in Figure 1-3 Edge Connector Dimensions of the Qseven™ Module from Pin 1 to Pin 2.

## Preface

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### Qseven™ Concept

The Qseven™ concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven™ modules have a standardized form factor of 70mm x 70mm and have specified pinouts based on the high speed MXM system connector that has a standardized pinout regardless of the vendor. The Qseven™ module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network and multiple USB ports. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven™ module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, Qseven™ applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class Qseven™ modules. Simply unplug one module and replace it with another, no redesign is necessary.

Qseven™ offers the newest I/O technologies on this minimum size form factor. This includes serial high speed buses such as:

- PCIexpress™
- ExpressCard™
- Serial ATA®
- Secure Digital I/O interface
- DisplayPort™, TMDS or SDVO Interface
- USB 2.0
- High Definition Digital Audio
- LPC interface
- Gigabit Ethernet
- LVDS Display Interface

Plus additional control and power management signals.

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## Intended Audience

This Qseven™ electromechanical specification is intended for technically qualified personnel. It is not intended for general audiences.

## Symbols

The following symbols may be used in this specification:



### **Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*



### **Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*



### **Note**

*Notes call attention to important information that should be observed.*

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## Lead-Free Designs (RoHS)

All Qseven™ designs shall be created from lead-free components in order to be RoHS compliant.

## Qseven™ Logo usage

The Qseven™ logo is freely available for members of the Qseven™ consortium. The logo can only be applied to products that are fully compliant to the latest specification of the Qseven™ standard.

High resolution formats are available at the members area [www.qseven-standard.org](http://www.qseven-standard.org).



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## Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express. Next-generation high speed serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
DDC	Display Data Channel is an I <sup>2</sup> C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
GBE	Gigabit Ethernet
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial interface standard for hard disks.
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
HDA	High Definition Audio
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
SMB	System Management Bus
LVDS	Low-Voltage Differential Signaling
ACPI	Advanced Control Programmable Interface
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EC.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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## 1 Qseven™ Mechanical Characteristics

The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

Edge-fingers on the module are referenced to the PCB slot center with an overall PCB thickness of  $1.2\text{mm} \pm 0.1$  measured across the fingers including the plating and/or metalization on both sides. Bevel is optional, but edge shall be free of burrs and shall not have sharp edges. The components located on the top side of the module are up to 5.5mm high. The bottom components have a maximum height of 2.5mm while the standard distance between the standard MXM connector on the carrier board and the Qseven™ module is 2.7mm. When using the standard MXM connector, with an overall height of 5.5mm, carrier board component placement below the Qseven module is not permitted.

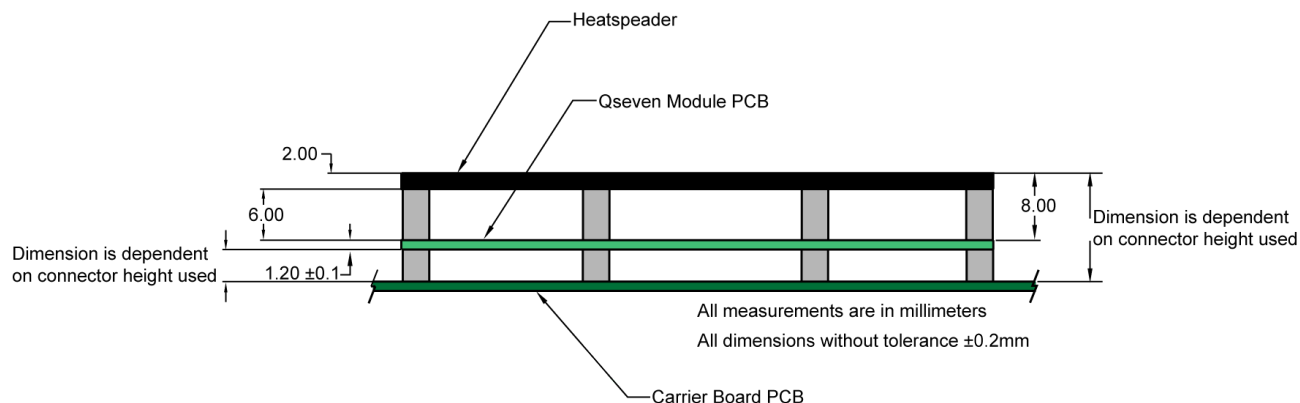
If it is necessary to place carrier board components below the Qseven module, then a MXM connector with an overall height of 7.8mm must be used and no carrier board component can exceed a maximum height of 2.5mm. Refer to section 1.3 regarding MXM connector specifications.

The heatspreader offered for Qseven™ modules acts as a thermal coupling device and is not a heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heatspreader. The dissipation of heat will fluctuate between different CPU boards. Refer to the Qseven™ module's user's guide for heatspreader dimensions and specifications.

The standoffs for the heatspreader and carrier board must not exceed 5.6mm overall external diameter. This ensures that the standoff contact area does not exceed the defined mounting hole footprint on the Qseven™ module. The screw that is to be used for mounting must be a metric thread M2.5 DIN7985 / ISO7045.

Qseven™ modules are defined to feature ultra low power CPU and chipset solutions with an ultra low "Thermal Design Power" (TDP). Furthermore, the modules power consumption should not exceed 12W.

**Figure 1-1 Overall Height including Heatspreader of the Qseven™ Module**



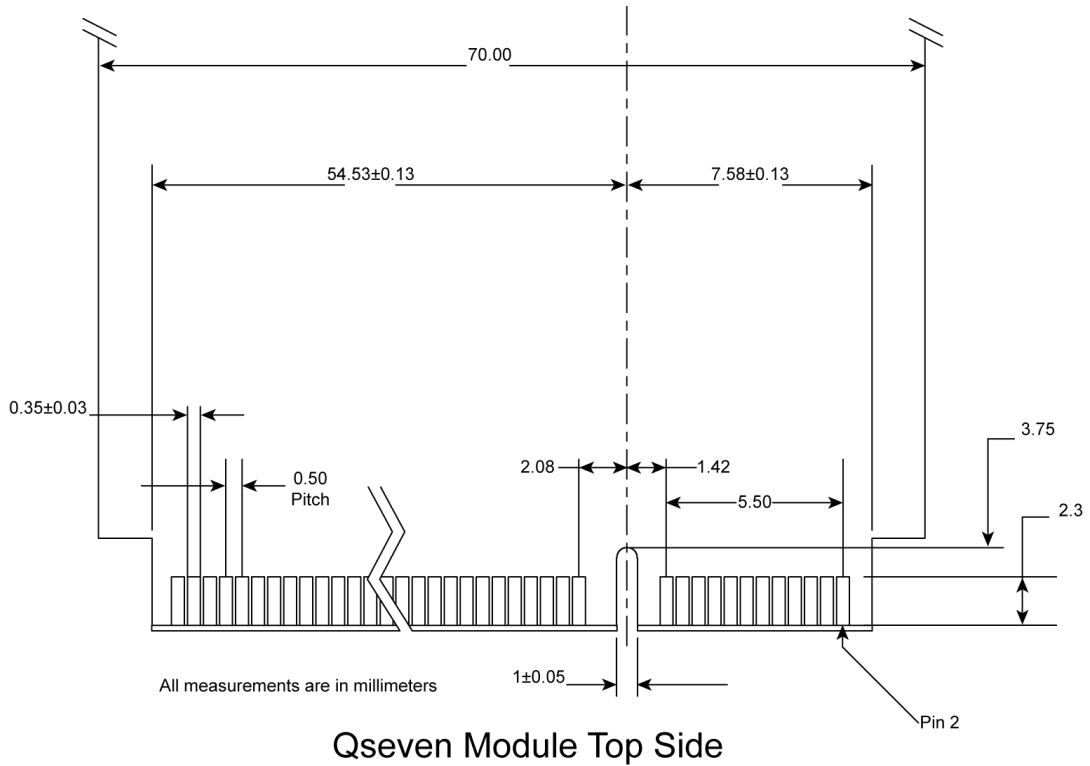
Rear View of Qseven Module



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## 1.1.2 Edge Connector Dimensions of the PCB

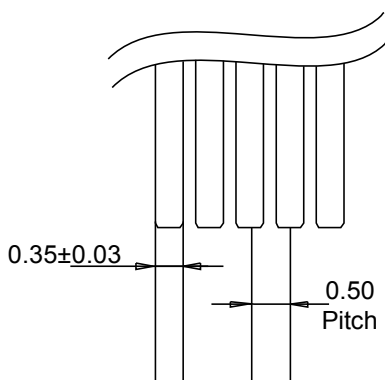
Figure 1-3 Edge Connector Dimensions of the Qseven™ Module



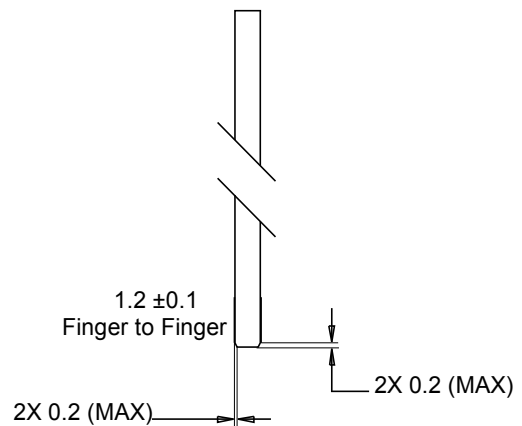
## 1.1.3 Single Edge Finger Dimensions

Figure 1-4 Edge Finger Dimensions of the Qseven™ Module

Edge Finger Top View



Edge Finger Side View



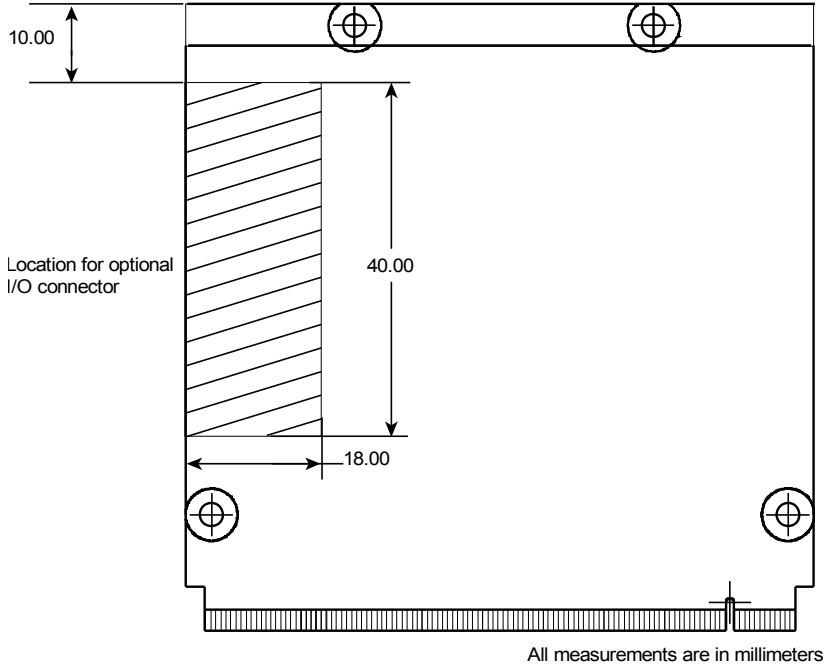
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## 1.1.4 Location for Optional I/O Connector

If an optional I/O connector, such as a Video Capture Port (VCP), is to be used it shall be placed in the I/O connector location area as defined in Figure 1-5.

This area is not a keep-out area and can be used for component placement if no additional I/O connector is required.

Figure 1-5 Optional I/O Connector Area



Qseven Module Top Side

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## 1.2 MXM Connector

The Qseven™ module utilizes a 230-pin card-edge connector that is also used for PCI Express capable notebook graphics cards following the MXM specification. Therefore, this connector type is also known as a MXM connector.

The MXM edge connector is the result of an extensive collaborative design effort with the industry's leading notebook manufacturers. This collaboration has produced a robust, low-cost edge connector that is capable of handling high-speed serialized signals.

The MXM connector accommodates various connector heights for different carrier board applications needs. This specification suggests two connector heights, 7.8mm and 5.5mm.

**Table 1-1 MXM Connector**

Manufacturer	Part Number	Specification	Resulting height between carrier board and Qseven™ module	Overall height of the MXM Connector
Foxconn	AS0B326-S55N-7F	AS0B326-S78N-7F	5.0mm	7.8mm
Foxconn	AS0B326-S78N-7F	AS0B326-S78N-7F	2.7mm	5.5mm
Speedtech		SPEC0378	5.0mm	7.8mm
Speedtech		SPEC0378	2.7mm	5.5mm
Lotes		SP-AAA-MXM-001	5.0mm	7.8mm
Lotes		SP-AAA-MXM-001	2.7mm	5.5mm

### 1.2.1 Environmental Characteristics

**Table 1-2 Environmental Characteristics for MXM Connectors**

Parameter	Specification
Durability	EIA-364-9 30 cycles
Mating and unmating force	EIA-364-13C LIF/angled insertion styled cards: Maximum insertion force: 1.3 kg Maximum extraction force: 1.6 kg  Slide-in/side insertion styled cards Maximum insertion force: 6.0 kg Maximum extraction force: 4.6 kg <i>Note: numbers tabulated using a velocity of 25 mm/min</i>
Vibration	EIA-364-28D – Test condition VII condition D With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB
Shock	EIA-364-27B – Test condition A With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB

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## 1.2.2 Electrical Characteristics

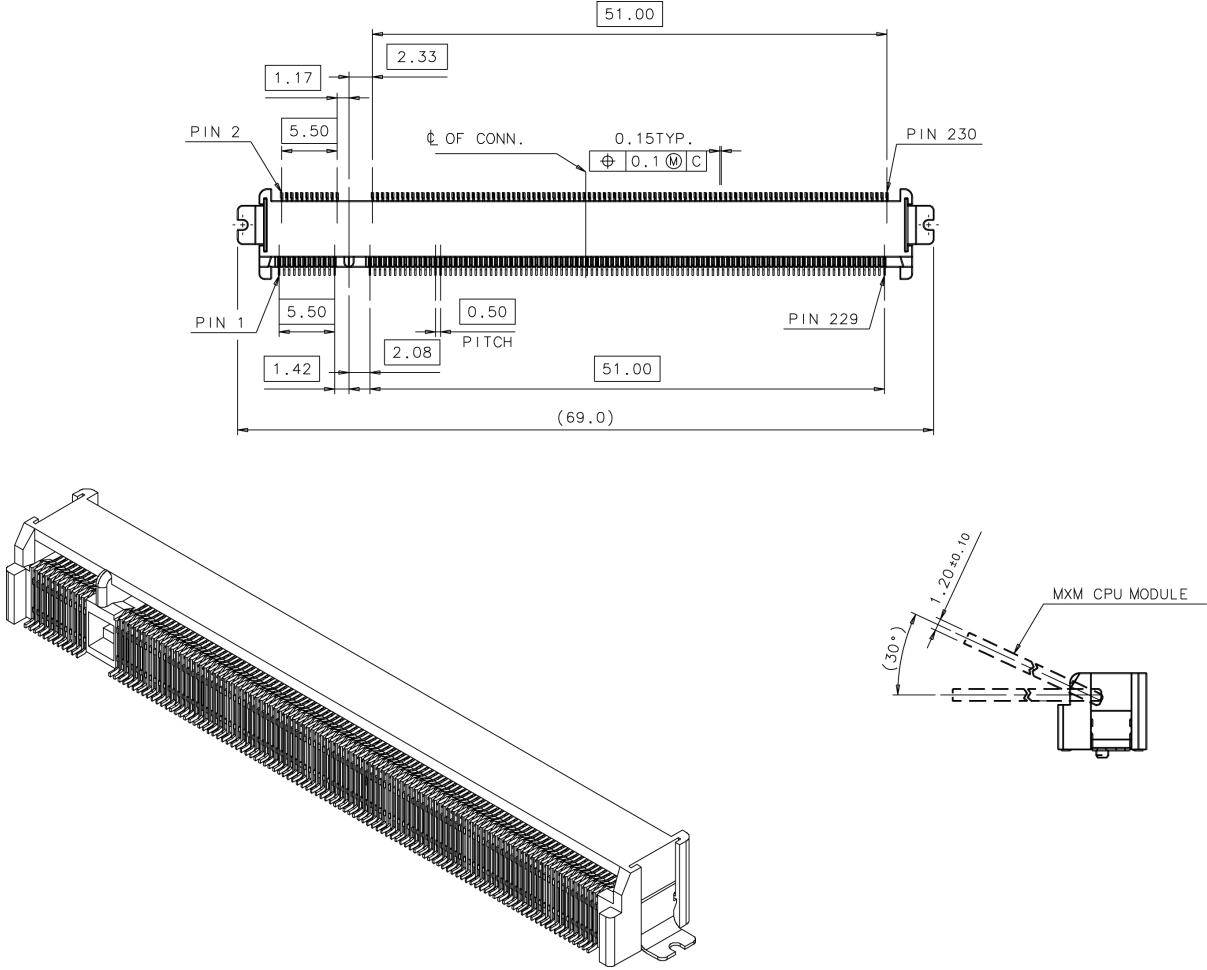
Table 1-3 Electrical Characteristics for MXM Connectors

Parameter	Specification
Low Level Contact Resistance	EIA-364-23B – Specify which option used. Do not use option 4. Requirement: 40 mΩ maximum for initial measurements 50 mΩ maximum or Delta R = 20 mΩ maximum, whichever is less, for measurements after other tests
Insulation Resistance	EIA-364-21C Requirements: Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B – Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 kV AC, (50 Hz) for 1 minute.
Current Rating	Current requirement: Pins rated for 0.5 Amp continuous The temperature rise above ambient shall not exceed 30 °C, where ambient condition is 25 °C still air.
Voltage Rating	50VDC per contact
Impedance	EIA-364-108 Impedance Requirements: 100 ± 20 Ω differential, 50 ± 10 Ω single ended.
Insertion Loss	EIA-364-101 Insertion Loss Requirements: 1 dB max up to 1.25 GHz; ≤ [1.6* (F-1.25)+1] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ 5 dB at F = 3.75 GHz) where F is frequency in GHz.
Return Loss	EIA-364-108 Return Loss Requirements: ≤ -12 dB up to 1.3 GHz ≤ -7dB up to 2 GHz ≤ -4 dB up to 3.75 GHz
Near End Crosstalk	EIA-364-90 Crosstalk(NEXT) Requirements: -32 dB max up to 1.25 GHz ≤ -[32 – 2.4* (F – 1.25)] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ -26 dB at F = 3.75 GHz) where F is frequency in GHz.

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## 1.2.3 MXM Connector Dimensions

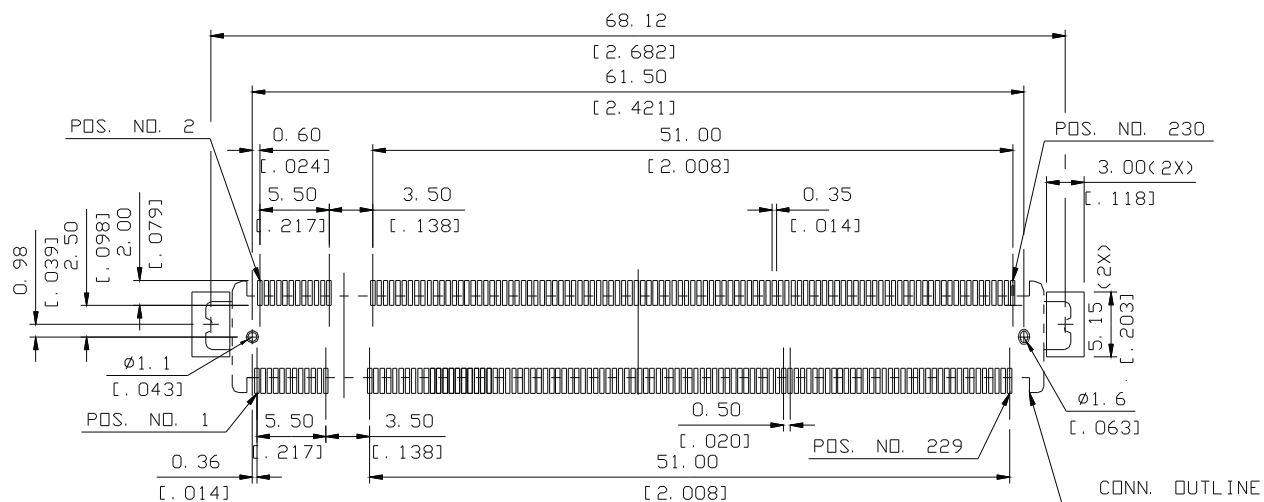
Figure 1-6 MXM Connector



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## 1.2.4 MXM Connector Footprint

Figure 1-7 Carrier Board PCB Footprint for the MXM Connector



## 2 Qseven™ Feature Overview

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The Qseven™ mandatory and optional features. Table 2-1 shows the minimum and maximum required configuration of the feature set.

**Table 2-1 Qseven™ Supported Features**

System I/O Interface	Minimum Configuration	Maximum Configuration
PCI Express lanes	2 (x1 link)	4
Serial ATA channels	0	2
USB 2.0 ports	4	8
LVDS channels	0	Dual Channel 24bits
DisplayPort, TMDS, SDVO	0	1
High Definition Audio	1	1
Gigabit Ethernet	0	1
ExpressCard support	0	2
Low Pin Count bus	1	1
Secure Digital I/O 8-bit for SD/MMC cards	0	1
System Management Bus	1	1
I <sup>2</sup> C Bus	1	1
Watchdog Trigger	1	1
Power Button	1	1
Power Good	1	1
Reset Button	1	1
LID Button	0	1
Sleep Button	0	1
Suspend To RAM (S3 mode)	0	1
Wake	0	1
Battery low alarm	0	1
Thermal control	0	1
FAN control	0	1

## 3 Connector Pin Assignments

There are 115 edge fingers on the top and bottom side of the Qseven™ module that mate with the MXM connector. Table 3-1 lists the pin assignments for all 230 edge fingers.

**Table 3-1 Connector Pinout Description**

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
	KEY		KEY
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	SDIO_PWRSEL
57	GND	58	GND
59	HDA_SYNC	60	SMB_CLK
61	HDA_RST#	62	SMB_DAT
63	HDA_BITCLK	64	SMB_ALERT#
65	HDA_SDI	66	I2C_CLK
67	HDA_SDO	68	I2C_DAT

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Pin	Signal	Pin	Signal
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7-	76	USB_P6-
77	USB_P7+	78	USB_P6+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5-	82	USB_P4-
83	USB_P5+	84	USB_P4+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CL_PRES	92	RSVD
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	LVDS_A0+	100	LVDS_B0+
101	LVDS_A0-	102	LVDS_B0-
103	LVDS_A1+	104	LVDS_B1+
105	LVDS_A1-	106	LVDS_B1-
107	LVDS_A2+	108	LVDS_B2+
109	LVDS_A2-	110	LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	LVDS_A3+	114	LVDS_B3+
115	LVDS_A3-	116	LVDS_B3-
117	GND	118	GND
119	LVDS_A_CLK+	120	LVDS_B_CLK+
121	LVDS_A_CLK-	122	LVDS_B_CLK-
123	LVDS_BLT_CTRL	124	RSVD
125	LVDS_DID_DAT	126	LVDS_BLC_DAT
127	LVDS_DID_CLK	128	LVDS_BLC_CLK
129	RSVD	130	RSVD
131	SDVO_BCLK+	132	SDVO_INT+
133	SDVO_BCLK-	134	SDVO_INT-
135	GND	136	GND
137	SDVO_GREEN+	138	SDVO_FLDSTALL+
139	SDVO_GREEN-	140	SDVO_FLDSTALL-
141	GND	142	GND
143	SDVO_BLUE+	144	SDVO_TVCLKIN+
145	SDVO_BLUE-	146	SDVO_TVCLKIN-
147	GND	148	GND
149	SDVO_RED+	150	SDVO_CTRL_DAT
151	SDVO_RED-	152	SDVO_CTRL_CLK

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Pin	Signal	Pin	Signal
153	HDMI_HPD#	154	DP_HPD#
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	EXCD0_PERST#	172	EXCD1_PERST#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	EXCD0_CPPE#	178	EXCD1_CPPE#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR
195	FAN_TACHOIN	196	FAN_PWMOUT
197	GND	198	GND
199	RSVD	200	RSVD
201	RSVD	202	RSVD
203	RSVD	204	RSVD
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

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## 3.1 Signal Descriptions

The “#” symbol at the end of the signal name indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level. Differential pairs are indicated by trailing '+' and '-' signs for the positive or negative signal. All required pull-ups or pull-down resistors shall be implemented on the Qseven™ module. This ensures that none of the signals that are not used will be left floating.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

**Table 3-2 Signal Terminology**

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
I <sub>OL</sub>	Output low current The I <sub>OL</sub> is the maximum output low current the module must be able to drive to an external circuitry.
I <sub>IL</sub>	Input low current The I <sub>IL</sub> is the maximum input low current that must be provided to the Qseven module via external circuitry in order to guarantee a proper logic low level of the signal.
P	Power Input
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.1.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

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## 3.1.1 PCI Express Interface Signals

Table 3-3 Signal Definition PCI Express

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	PCIE		I
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	PCIE		O
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	PCIE		I
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	PCIE		O
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	PCIE		I
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	PCIE		O
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	PCIE		I
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	PCIE		O
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	PCIE		O
PCIE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	CMOS 3.3V Suspend	≥ 5 mA	I
PCIE_RST#	Reset Signal for external devices.	CMOS 3.3V	max 1 mA	O

### Note

There are a total of 4 PCI Express TX and RX differential pairs supported on the Qseven™ module. Depending on the features supported by the Qseven™ module and the core logic chipset used, these lines may be used to form x1 or x4 PCI Express links. The documentation for the Qseven™ module shall clearly identify, which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

## 3.1.2 ExpressCard Support Pins

Table 3-4 Signal Definition ExpressCard

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
EXCD0_CPPE#	ExpressCard slot #0 capable card request.	CMOS 3.3V	≥ 5 mA	I
EXCD0_PERST#	ExpressCard slot #0 reset.	CMOS 3.3V	max. 1 mA	O
EXCD1_CPPE#	ExpressCard slot #1 capable card request.	CMOS 3.3V	≥ 5 mA	I
EXCD1_PERST#	ExpressCard slot #1 reset.	CMOS 3.3V	max. 1 mA	O

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## 3.1.3 Gigabit Ethernet Signals

Table 3-5 Signal Definition Ethernet

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
GBE_MDI0+ GBE_MDI0-	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI1+ GBE_MDI1-	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI2+ GBE_MDI2-	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_MDI3+ GBE_MDI3-	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_CTREF	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		
GBE_LINK#	Ethernet controller 0 link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_LINK100#	Ethernet controller 0 100Mbit/sec link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_LINK1000#	Ethernet controller 0 1000Mbit/sec link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_ACT#	Ethernet controller 0 activity indicator, active low.	CMOS 3.3V OD	max 10 mA	O

## 3.1.4 Serial ATA Interface Signals

Table 3-6 Signal Definition SATA

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	SATA		I
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	SATA		O
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	SATA		I
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	SATA		O
SATA_ACT#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	max. 10mA	O

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## 3.1.5 USB Interface Signals

Table 3-7 Signal Definition USB

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
USB_P0+ USB_P0-	Universal Serial Bus Port 0 differential pair.	USB		I/O
USB_P1+ USB_P1-	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	USB		I/O
USB_P2+ USB_P2-	Universal Serial Bus Port 2 differential pair.	USB		I/O
USB_P3+ USB_P3-	Universal Serial Bus Port 3 differential pair.	USB		I/O
USB_P4+ USB_P4-	Universal Serial Bus Port 4 differential pair.	USB		I/O
USB_P5+ USB_P5-	Universal Serial Bus Port 5 differential pair.	USB		I/O
USB_P6+ USB_P6-	Universal Serial Bus Port 6 differential pair.	USB		I/O
USB_P7+ USB_P7-	Universal Serial Bus Port 7 differential pair.	USB		I/O
USB_0_1_OC#	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_2_3_OC#	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_4_5_OC#	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_6_7_OC#	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_CL_PRES	USB client present detect pin. The USB port 1 may operate as USB client or USB host. If USB port 1 is configured as client port then this pin indicates that an external USB host is connected to USB port 1.	CMOS 3.3V	≥ 5 mA	I

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## 3.1.6 SDIO Interface Signals

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories.

**Table 3-8 Signal Definition SDIO**

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	CMOS 3.3V		I/O
SDIO_CLK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	CMOS 3.3V		O
SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	CMOS 3.3V OD/PP		I/O
SDIO_LED	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	CMOS 3.3V	max 1 mA	O
SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	CMOS 3.3V		O
SDIO_PWR#	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	CMOS 3.3V		O
SDIO_PWRSEL	SDIO Power Select. This signal is used to select the power source for an external SD/MMC socket.	CMOS 3.3V		O
SDIO_DAT0-7	SDIO Data lines. These signals operate in push-pull mode.	CMOS 3.3V PP		I/O

## 3.1.7 High Definition Audio Signals

**Table 3-9 Signal Definition HDA**

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
HDA_RST#	HD Audio Codec Reset.	CMOS 3.3V		O
HDA_SYNC	Serial Bus Synchronization.	CMOS 3.3V		O
HDA_BCLK	HD Audio 24 MHz Serial Bit Clock from Codec.	CMOS 3.3V		O
HDA_SDO	HD Audio Serial Data Output to Codec.	CMOS 3.3V		O
HDA_SDIN	HD Audio Serial Data Input from Codec.	CMOS 3.3V		I

### Note

*The High Definition Audio interface found on the Qseven module complies with Intel® High Definition Audio Specification 1.0*

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## 3.1.8 LVDS Flat Panel Signals

Table 3-10 Signal LVDS

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
LVDS_PPEN	Controls panel power enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLEN	Controls panel Backlight enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLT_CTRL	Controls the panel backlight brightness via pulse width modulation (PWM)	CMOS 3.3V		O
LVDS_A0+ LVDS_A0-	LVDS primary channel differential pair 0.	LVDS		O
LVDS_A1+ LVDS_A1-	LVDS primary channel differential pair 1.	LVDS		O
LVDS_A2+ LVDS_A2-	LVDS primary channel differential pair 2.	LVDS		O
LVDS_A3+ LVDS_A3-	LVDS primary channel differential pair 3.	LVDS		O
LVDS_A_CLK+ LVDS_A_CLK-	LVDS primary channel differential pair clock lines.	LVDS		O
LVDS_B0+ LVDS_B0-	LVDS secondary channel differential pair 0.	LVDS		O
LVDS_B1+ LVDS_B1-	LVDS secondary channel differential pair 1.	LVDS		O
LVDS_B2+ LVDS_B2-	LVDS secondary channel differential pair 2.	LVDS		O
LVDS_B3+ LVDS_B3-	LVDS secondary channel differential pair 3.	LVDS		O
LVDS_B_CLK+ LVDS_B_CLK-	LVDS secondary channel differential pair clock lines.	LVDS		O
LVDS_DID_CLK	DisplayID DDC clock line used for LVDS flat panel detection.	CMOS 3.3V OD		I/O
LVDS_DID_DAT	DisplayID DDC data line used for LVDS flat panel detection.	CMOS 3.3V OD		I/O
LVDS_BLC_CLK	Control clock signal for external SSC clock chip.	CMOS 3.3V OD		I/O
LVDS_BLC_DAT	Control data signal for external SSC clock chip.	CMOS 3.3V OD		I/O

### Note

*The LVDS flat panel configuration within the BIOS of the Qseven™ module shall be implemented in accordance to the DisplayID specification that is under development within the Video Electronics Standards Association (VESA). For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA).*

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## 3.1.9 SDVO Interface Signals

The Intel® SDVO port is the second generation of digital video output offered by compliant Intel® Graphics Memory Controller Hubs (GMCH). The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependent upon the active display resolution and timing. Essentially, an SDVO port will transmit display data in a high-speed, serial format across differential AC coupled signals. A SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

The SDVO port provides a two-wire point-to-point communication path between the SDVO device and the Intel GMCH. The SDVO control clock and data provide similar functionality to I<sup>2</sup>C. However unlike I<sup>2</sup>C, this interface is intended to be point-to-point and will require the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1MHz) than a traditional I<sup>2</sup>C interface would.

The SDVO device accepts this serialized format and then translates the data into the appropriate display format. SDVO devices are third party codec's that utilize the SDVO port as an input and may have a variety of output formats, including DVI, LVDS, HDMI, TV-Out.

**Table 3-11 Signal Definition SDVO**

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
SDVO_BCLK- SDVO_BCLK+	SDVO differential pair clock lines.	PCIE		O
SDVO_INT- SDVO_INT+	SDVO differential pair interrupt input lines.	PCIE		I
SDVO_GREEN- SDVO_GREEN+	SDVO differential pair green data lines.	PCIE		O
SDVO_BLUE- SDVO_BLUE+	SDVO differential pair blue data lines.	PCIE		O
SDVO_RED- SDVO_RED+	SDVO differential pair red data lines.	PCIE		O
SDVO_FLDSTALL- SDVO_FLDSTALL+	SDVO differential pair field stall lines.	PCIE		I
SDVO_TVCLKIN- SDVO_TVCLKIN+	SDVO differential pair TV-Out synchronization clock lines.	PCIE		I
SDVO_CTRL_CLK	I <sup>2</sup> C based control signal (clock) for SDVO device. <b>Note:</b> If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.	CMOS 3.3V OD		I/O
SDVO_CTRL_DAT	I <sup>2</sup> C based control signal (data) for SDVO device. <b>Note:</b> If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.	CMOS 3.3V OD		I/O

### Note

*Support of the SDVO interface is chipset dependent and therefore may not be available on all Qseven modules. The SDVO interface signals are shared with the signals for the DisplayPort interface and/or the TMDS interface.*

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## 3.1.10 DisplayPort Interface Signals

DisplayPort is an open, industry standard digital display interface, that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

**Table 3-12 Signal Definition DisplayPort**

Signal	Shared With	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
DP_LANE3- DP_LANE3+	SDVO_BCLK- SDVO_BCLK+	DisplayPort differential pair lines lane 3.	PCIE		O
DP_LANE2- DP_LANE2+	SDVO_BLUE- SDVO_BLUE+	DisplayPort differential pair lines lane 2.	PCIE		O
DP_LANE1- DP_LANE1+	SDVO_GREEN- SDVO_GREEN+	DisplayPort differential pair lines lane 1.	PCIE		O
DP_LANE0- DP_LANE0+	SDVO_RED- SDVO_RED+	DisplayPort differential pair lines lane 0.	PCIE		O
DP_AUX- DP_AUX+	SDVO_FLDSTALL- SDVO_FLDSTALL+	Auxiliary channel used for link management and device control. Differential pair lines.	PCIE		I/O
DP_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

 **Note**

*Support of the DisplayPort interface is chipset dependent and therefore may not be available on all Qseven modules. The DisplayPort interface signals are shared with the signals for the SDVO interface and/or the TMDS interface.*

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## 3.1.11 HDMI Interface Signals

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Both HDMI and DVI were pioneered by Silicon Image and are based on TMDS®, Silicon Image's powerful, high-speed, serial link technology.

**Table 3-13 Signal Definition HDMI**

Signal	Shared With	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
TMDS_CLK- TMDS_CLK+	SDVO_BCLK- SDVO_BCLK+	TMDS differential pair clock lines.	TMDS		O
TMDS_LANE0- TMDS_LANE0+	SDVO_BLUE- SDVO_BLUE+	TMDS differential pair lines lane 0.	TMDS		O
TMDS_LANE1- TMDS_LANE1+	SDVO_GREEN- SDVO_GREEN+	TMDS differential pair lines lane 1.	TMDS		O
TMDS_LANE2- TMDS_LANE2+	SDVO_RED- SDVO_RED+	TMDS differential pair lines lane 2.	TMDS		O
HDMI_CTRL_CLK	SDVO_CTRL_CLK	DDC based control signal (clock) for HDMI device. <b>Note:</b> Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.	CMOS 3.3V OD		I/O
HDMI_CTRL_DAT	SDVO_CTRL_DAT	DDC based control signal (data) for HDMI device. <b>Note:</b> Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.	CMOS 3.3V OD		I/O
HDMI_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

### Note

*Support of the TMDS interface is chipset dependent and therefore may not be available on all Qseven modules. The TMDS interface signals are shared with the signals for the SDVO interface and/or the DisplayPort interface.*

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## 3.1.12 LPC Interface Signals

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy devices such as a Super I/O controller or a firmware hub device.

**Table 3-14 Signal Definition LPC**

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
LPC_AD[0..3]	Multiplexed Command, Address and Data.	CMOS 3.3V		I/O
LPC_FRAME#	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	CMOS 3.3V		O
LPC_LDRQ#	LPC DMA request.	CMOS 3.3V		I
LPC_CLK	LPC clock.	CMOS 3.3V		O
SERIRQ	Serialized Interrupt.	CMOS 3.3V		I/O

## 3.1.13 Input Power Pins

**Table 3-15 Signal Definition Input Power**

Signal	Description	I/O
VCC	Power Supply +5VDC ±5%.	P
VCC_5V_SB	Standby Power Supply +5VDC ±5%.	P
VCC_RTC	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P
GND	Power Ground.	P

## 3.1.14 Power Control Signals

**Table 3-16 Signal Definition Power Control**

Signal	Description of Power Control signals	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
PWGIN	High active input for the Qseven™ module indicates that power from the power supply is ready.	CMOS 5V	≥ 4 mA	I
PWRBTN#	Power Button: Low active power button input. This signal is triggered on the falling edge.	CMOS OD 3.3V Standby	≥ 10 mA	I

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## 3.1.15 Power Management Signals

Table 3-17 Signal Definition Power Management

Signal	Description of Power Management signals	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
RSTBTN#	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven module.	CMOS OD 3.3V	≥ 10 mA	I
BATLOW#	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	CMOS OD 3.3V Suspend	≥ 10 mA	I
WAKE#	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	CMOS OD 3.3V Suspend	≥ 10 mA	I
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S3#	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S5#	S5 State: This signal indicates S4 or S5 (Soft Off) state.	CMOS 3.3V Suspend	max. 1 mA	O
SLP_BTN#	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	CMOS OD 3.3V Suspend	≥ 10 mA	I
LID_BTN#	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. TBD: Open/Close state.	CMOS OD 3.3V Suspend	≥ 10 mA	I

 **Note**

*It must be guaranteed that all the carrier board power rails, that are generated out of the VCC power rail, will be enabled by the SUS\_S3# signal.*

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## 3.1.16 Miscellaneous Signals

Table 3-18 Signal Definition Miscellaneous

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
WDTRIG#	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse.	CMOS OD 3.3V	≥ 10 mA	I
WDOUT	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	CMOS 3.3V	max. 5 mA	O
I2C_CLK	Clock line of I <sup>2</sup> C bus.	CMOS 3.3V OD		I/O
I2C_DAT	Data line of I <sup>2</sup> C bus.	CMOS 3.3V OD		I/O
SMB_CLK	Clock line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_DAT	Data line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_ALERT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	CMOS 3.3V OD Suspend		I/O
SPKR	Output for audio enunciator, the “speaker” in PC AT systems	CMOS 3.3V		O
BIOS_DISABLE#	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations.	CMOS 3.3V		I
MFG_NC0 MFG_NC1 MFG_NC2 MFG_NC3	Do not connect on the carrier board. These pins are reserved for manufacturing purposes.	n.a.	n.a.	n.a.
RSVD	Do not connect.			NC

## 3.1.17 Thermal Management Signals

Table 3-19 Signal Definition Thermal Management

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
THRM#	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	CMOS 3.3V		I

## 3.1.18 Fan Control Implementation

Table 3-20 Signal Definition Fan Control

Signal	Description	I/O Type	I <sub>OL</sub> /I <sub>IL</sub>	I/O
FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature.	CMOS 3.3V OC		O
FAN_TACHOIN	Fan tachometer input.	CMOS 3.3V		I

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## 3.2 Input Power Requirements

Qseven™ modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by Qseven™ to provide a +5V standby voltage on the Qseven™ module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. The same applies to the +3V RTC battery voltage. If no RTC/CMOS backup functionality is required by the system, then the +3V RTC supply battery voltage can be omitted.

**Table 3-21 Input Power Characteristics**

Power Rail	Nominal Input	Input Range	Max Input Ripple
VCC	+5V	+4.75V - +5.25V	±50 mV
VCC_5V_SB	+5V	+4.75V - +5.25V	±50 mV
VCC_RTC	+3V	+2.0V - +3.3V	±20 mV

### Note

*If the standby 5V power rail 'VCC\_5V\_SB' is not provided by the carrier board, then all pins must be connected together with the standard 5V power rail 'VCC'.*

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## 3.2.1 Input Power Sequencing

Qseven input power sequencing requirements are as follows:

### Start Sequence:

- VCC\_RTC must come up at the same time or before VCC\_5V\_SB comes up.
- VCC\_5V\_SB must come up at the same time or before VCC comes up.
- PWGIN must be active at the same time or after VCC comes up.

### Stop Sequence:

- PWGIN must be inactive at the same time or before VCC goes down
- VCC must go down at the same time or before VCC\_5V\_SB goes down
- VCC\_5V\_SB must go down at the same time or before VCC\_RTC goes down

Figure 3-1 Input Power Sequencing

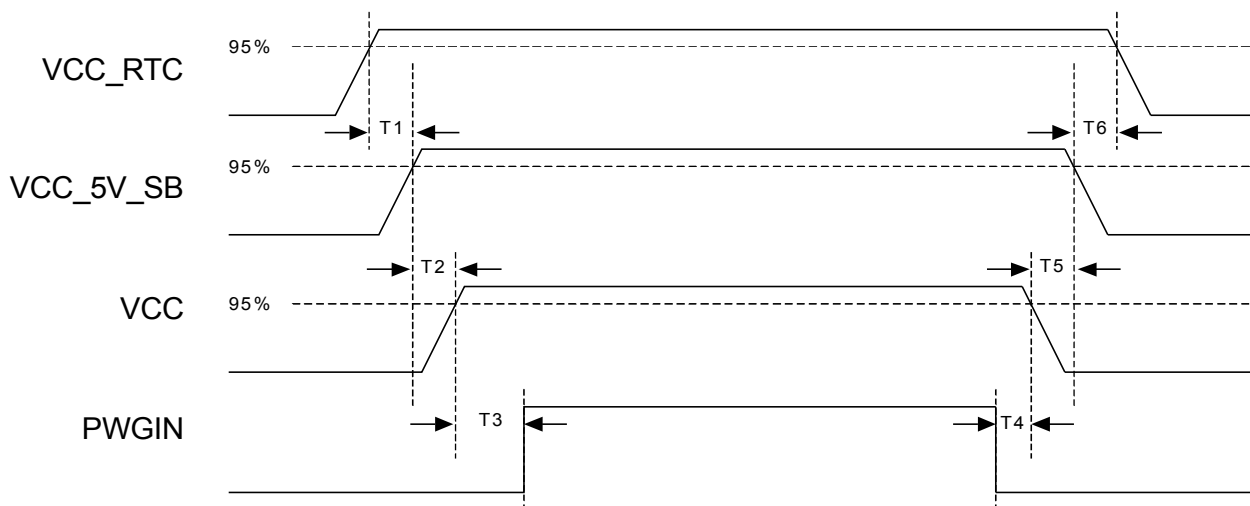


Table 3-22: Input Power Sequencing

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms
T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

## 4 Qseven™ Signaling Budgets

### 4.1 PCI Express

According to the PCI Express Base Specification Revision 1.1, a total available interconnect loss budget of 13.2 dB is allowed between the PCI Express host device on the Qseven™ CPU module and the PCI Express device on the carrier board, ExpressCard or PCI Express add-in card.

The electrical characteristic of the Qseven™ module is defined in terms of electrical insertion loss budgets. This budget allocation decouples the electrical specification for the carrier board designer and the Qseven™ module vendor. Unless otherwise noted, the specifications contained herein apply to all high-speed signals of each interface width definition. The signaling rate for encoded data is 2.5 Gigabit transfers/s and the signaling is point-to-point.

#### 4.1.1 Qseven™ Module PCI Express Budget Allocation

Figure 4-1 PCI Express Budget Allocation

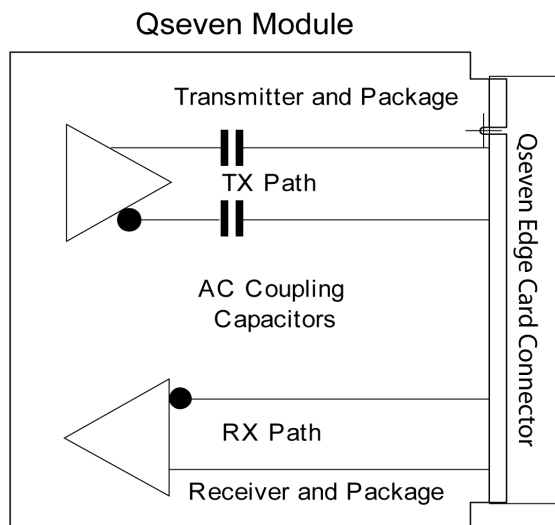


Table 4-1 PCI Express Budget Allocation

Segment	Loss Budget Value at 1.25 GHz	max. Trace Length	Comments
Qseven Module (TX path)	< 2.5 dB	2 inches	Note 1, 2, 3, 4, 5, 6
Qseven Module (RX path)	< 2.1 dB	2 inches	Note 1, 2, 4, 5, 6

#### Notes



1. The PCI Express Base Specification allows an interconnect loss of 13.2 dB for 1.25 GHz signals. The allocated Qseven™ loss budget does not include crosstalk and impedance mismatch. As a guide for design and simulation, the PCI Express CEM Specification recommends to subtract 5.2 dB from the 13.2 dB budget, to cover crosstalk and impedance mismatch for the total interconnect

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*path. The 5.2dB budget also includes the overall 1.25dB guard band as recommended by the PCI CEM Specification.*

- 2. This budget also includes the connector on the carrier board. The budget allocated to the Qseven™ connector is 1.0dB @ 1.25GHz.*
- 3. The TX path budget includes the additional damping of the DC decoupling capacitors.*
- 4. Typical damping of the PCB trace of 0.35dB/inch @ 1.25GHz (common value for FR-4 based material).*
- 5. Maximum 2 vias per trace for a RX path and maximum 4 vias per trace for a TX path on the connection from the core logic chipset to the Qseven™ connector on the Qseven™ module.*
- 6. Trace routing is implemented according to the design rules for high speed differential traces.*

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## 4.1.2 PCI Express Insertion Loss Budget

Figure 4-2 PCI Express Link Topology 1

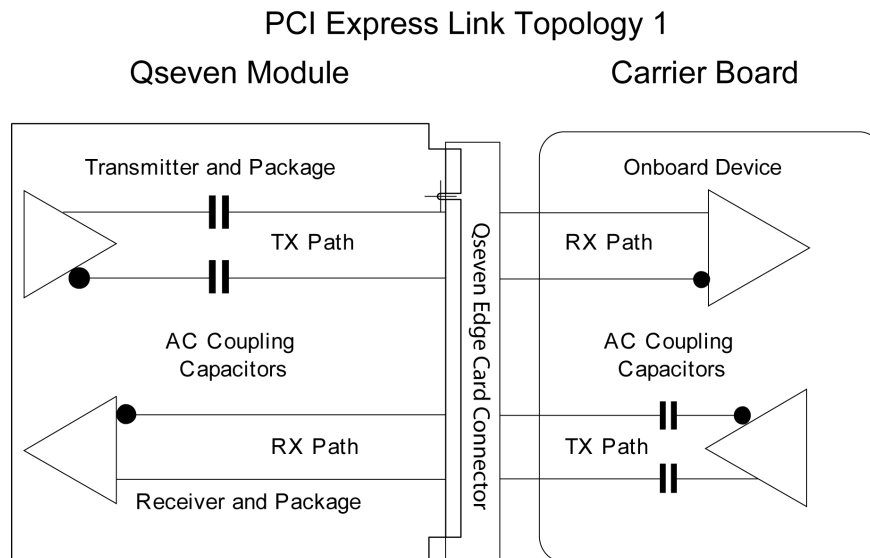
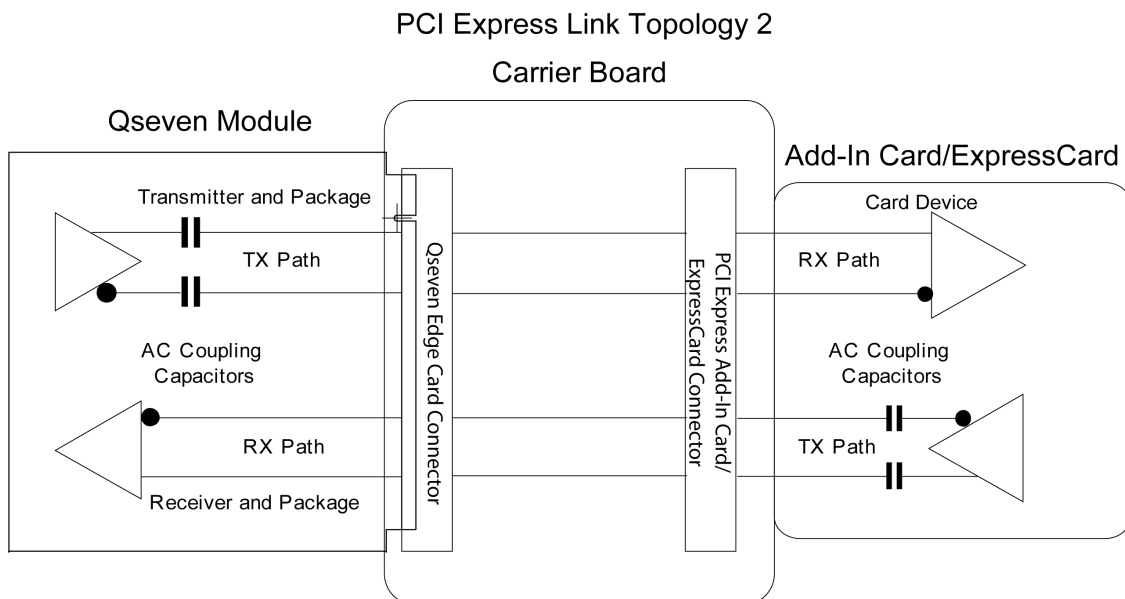


Figure 4-3 PCI Express Link Topology 2



 **Note**

The term “TX-path” that is used in Table 4-2 refers to the signal path from the PCI Express transmitter on the Qseven™ module to the PCI Express receiver, of an onboard device or on an add-in card, on the Qseven™ carrier board.

The term “RX-path” that is used in Table 4-2 refers to the signal path from the PCI Express transmitter, of an onboard device or on an add-in card on the Qseven™ carrier board, to the PCI Express receiver on the Qseven™ module.

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**Table 4-2 Carrier Board PCI Express Insertion Loss Budget**

Segment	Loss Budget Value at 1.25 GHz (dB)	max. Trace Length	Comments
Carrier Board Topology 1 (TX path)	5.5dB	14.5 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 1 (RX path)	5.9dB	15.7 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 2 (TX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard
Carrier Board Topology 2 (RX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard

The trace lengths presented in Table 4-2 are based on the following assumptions:

- Typical damping of the PCB trace of 0.35dB/inch @ 1,25GHz (common value for FR-4 based material)
- The RX path budget includes the additional damping of the DC decoupling capacitors and 2 additional vias for connecting the decoupling capacitors
- Maximum 2 vias per trace for a RX path and maximum 4 vias per trace for a TX path on the connection from the the Qseven™ connector on the Qseven™ carrier board to an onboard device
- Maximum 2 vias per trace for a RX path and maximum 2 vias per trace for a TX path on the connection from the Qseven™ connector on the Qseven™ carrier board to a PCI Express extension socket that is compliant to the properties defined in the PCI Express Card Electromechanical Specification (this includes standard PCI Express cards as well as ExpressCards).
- Trace routing is implemented according to the design rules for high speed differential traces.

The values in Table 4-2 are derived from a signal integrity simulation and reflect a worst case scenario. The values given are design rules for a maximum interoperability between Qseven™ modules from different vendors and customer specific Qseven™ carrier boards and shall be observed. Designers that face the necessity to deviate from the given values have to conduct a suitable signal integrity simulation to guarantee compliance to the Qseven™ specification and the underlying PCI Express specification. Carrier boards that do not follow the design rules presented in this specification and those that have not been simulated are not considered Qseven™ compliant.

For carrier board designers that want to set up a simulation environment they should contact their Qseven™ module vendor to obtain an Qseven™ module model for signal integrity simulation.

## Note

*Design guidelines for high speed differential traces can be found in the Qseven™ Design Guide.*

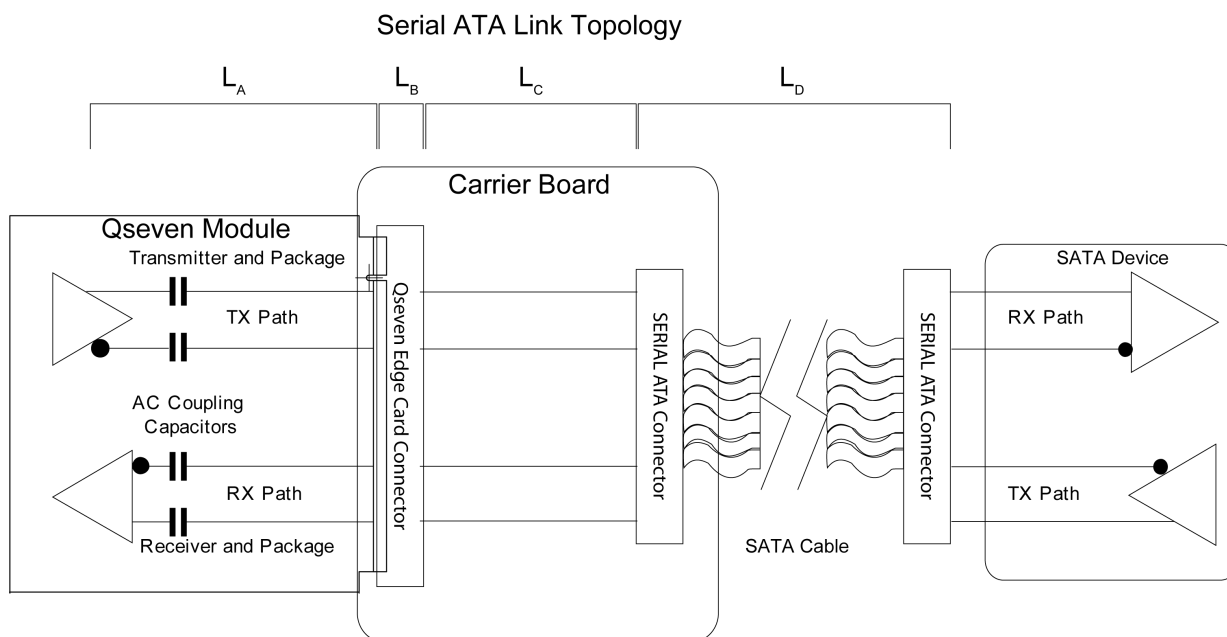
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## 4.2 Serial ATA

### 4.2.1 Serial ATA Insertion Loss Budget

As outlined in the Serial ATA Specification, the following insertion loss budgets for the SATA implementation on the Qseven™ module and carrier board shall be observed. Figure 4-4 shows a typical Serial ATA link topology of a Qseven™ based application.

**Figure 4-4 Serial ATA Link Topology**



**Table 4-3 SATA Loss Budget Allocation**

Segment	Loss Budget Value at 1.5 GHz (dB)	Max. Trace Length	Comments
$L_A$	1.05 dB	2.5 inches	Module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40 dB		
$L_B$	0.40 dB		MXM connector @ 1.5GHz
$L_C$	3.07 dB	7.2	Carrier Board trace @ 0.28 dB / GHz / inch
$L_D$	6.00 dB		Source specification cable and cable connector allowance
Total	10.92 dB		

The trace lengths presented in Table 4-3 are based on the following assumptions:

- Typical damping of the PCB trace of 0.42dB/inch @ 1,5GHz (common value for FR-4 based material)
- The budget includes the additional damping of the DC decoupling and the Qseven™ connector losses.
- Trace routing is implemented according to the design rules for high speed differential traces.

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## 4.3 USB

### 4.3.1 USB Insertion Loss Budget

Figure 4-5 USB Link Topology

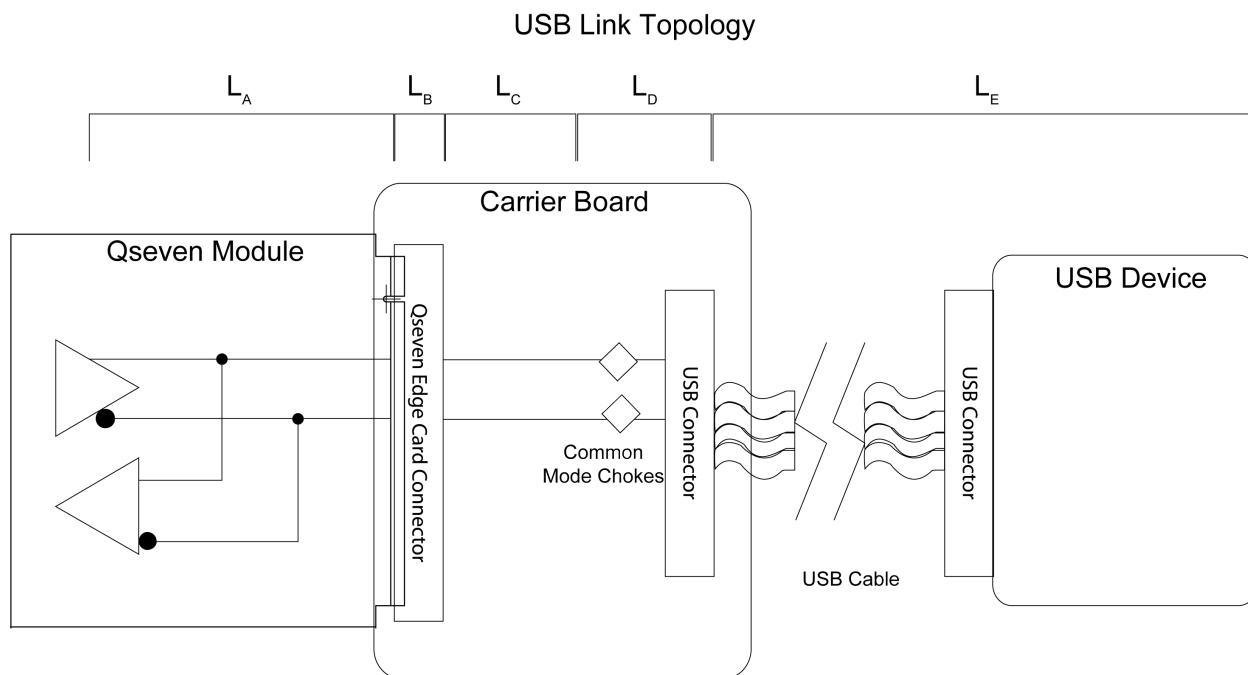


Table 4-4 USB Loss Budget Allocation

Segment	Loss Budget Value at 400 MHz	max. Trace Length	Comments
$L_A$	0.67 dB	6 inches	Module trace @ 0.28 dB / GHz / inch
$L_B$	0.05 dB		MXM connector at 400 MHz
$L_C$	1.68 dB	14 inches	Carrier Board trace @ 0.28 dB / GHz / inch
$L_D$	1.00 dB		USB connector and ferrite loss
$L_E$	5.80 dB		USB cable and far end connector loss, per source specification
Total	9.2 dB		

Qseven USB implementations should conform to insertion loss values less than or equal to those shown in Table 4-4 above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

“Device Down” implementations, in which the USB target device is implemented on the carrier board, may add the ferrite and USB connector insertion loss values to the carrier board budget.

The carrier board insertion loss budget then becomes  $L_C + L_D$ , or 2.68 dB.

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## 4.4 Gigabit Ethernet

### 4.4.1 Gigabit Ethernet Insertion Loss Budget

Figure 4-6 Gigabit Ethernet Link Topology

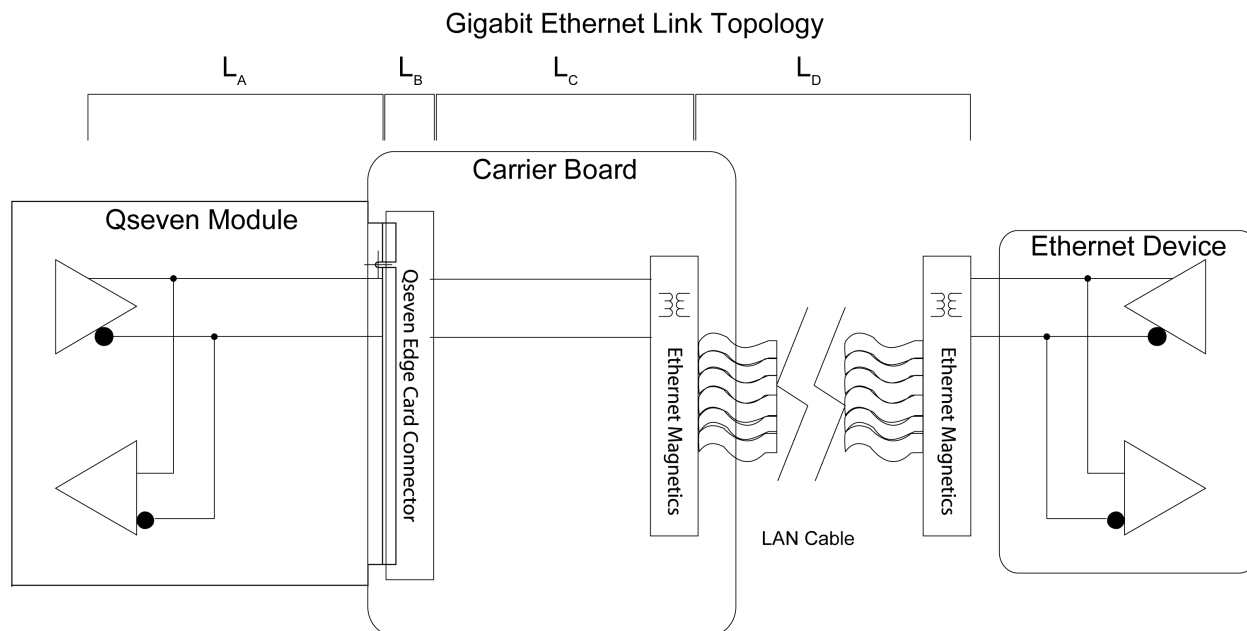


Table 4-5 Gigabit Ethernet Loss Budget Allocation

Segment	Loss Budget Value at 100 MHz	max. Trace Length	Comments
$L_A$	0.08 dB	2 inches	Module trace @ 0.28 dB / GHz / inch
$L_B$	0.02 dB		MXM connector at 100 MHz
$L_C$	0.15 dB	4 inches	Carrier Board trace @ 0.28 dB / GHz / inch
$L_D$	24.00 dB		Cable and cable connectors, integrated magnetics, per source spec
Total	24.25 dB		

Qseven Ethernet implementations should conform to insertion loss values less than or equal to those shown in Table 4-5 above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gigabit Ethernet specification.

“Device Down” implementations, in which the Ethernet target device is implemented on the carrier board (for instance, an Ethernet switch), may add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the carrier board budget. This insertion loss value is typically 1 dB. The carrier board insertion loss budget then becomes  $L_C + 1$  dB, or 1.15 dB.

## 5 Software Definitions

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### 5.1 BIOS Implementations

#### 5.1.1 LPC Super I/O Support

The Qseven™ BIOS firmware shall include integrated support for the following external LPC Super I/O controllers in order to provide additional legacy COM ports.

Support for the COM ports of the following Super I/Os shall be implemented in the Qseven™ module BIOS:

1. Winbond W83627HG LPC Super I/O with 2 COM ports
2. SMSC SCH3114 LPC Super I/O with 4 COM ports

If any of the additional functionality of the Super I/O is required by the application, then it may be implemented via the application's software program. There are Super I/O functions that can be configured by hardware straps, which is defined within the datasheet of that particular Super I/O (for example PS/2 keyboard functionality). By default, these functions must be disabled if the Super I/O is to be implemented on a Qseven™ module.

The base address for these Super I/O controllers shall be 0x2E to be sure that the legacy COM port devices of the Super I/O controller can be initialized by the BIOS.

## 5.2 Embedded Application Software Interface

### 5.2.1 General Information

Qseven™ embedded computer modules are equipped with additional functions for industrial applications. These functions are provided through the use of an API (Application Program Interface) called Embedded Application Software Interface (EASI). This API is provided via a shared library (for instance the `easi.dll` for Windows). Examples of this include Watchdog Timer, I<sup>2</sup>C Bus, LCD brightness control, BIOS user storage area and the reading of system temperatures. Due to the fact that no standardized software interface for these functions has been defined to date, the theoretical exchangeability of COMs has in practice proven to be more difficult than expected. In order to generally avoid the software modifications that such situations would require, the Qseven™ specification includes a consistent software API. Qseven™ modules from different manufacturers can thus be easily exchanged without modifications to hardware or software.

The API, which is provided by the module manufacturer, should contain the following files:

Operating System	EASI Files
Windows Vista 32	<code>easi.dll</code> , <code>easi.h</code>
Windows XP	<code>easi.dll</code> , <code>easi.h</code>
Windows XP Embedded	<code>easi.dll</code> , <code>easi.h</code>
Windows CE	<code>easi.dll</code> , <code>easi.h</code>
Linux	<code>easi.so</code> , <code>easi.h</code>

The above list only includes the most common operating systems but module manufacturers may provide API support for additional operating systems.

#### General rules for using EASI:

- *dwID* is the designator used to point to the target device that the function applies to, for example the primary I<sup>2</sup>C Bus. All *dwID* are 0-based identifiers that should be 0 unless other options are listed. If an undefined *dwID* value is passed to a given function, then the function should set the `EASI_STATUS_INVALID_PARAMETER` error.
- All version numbers are unsigned long integers where bits 31..24 represent major, 23..16 represent minor and 15..0 represent build number.
- Unless otherwise explicitly stated, the functions return 0 for failure and 1 for success. If a feature is not implemented then the function call must return a 0 to indicate failure.

The features described in the following sections are based on version 0.93 of EASI and shall be implemented by the Qseven™ module manufacturer.

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## 5.2.2 EASI Library

The library *EasiLibGetVersion* call can be used to determine the version of the interface and therefore its capabilities.

```
unsigned long EasiLibGetVersion(void);
```

Additionally, the *EasiLibGetLastError* call provides information about the status of the last library access by using one of the following values:

```
unsigned long EasiLibGetLastError(void);
```

```
#define EASI_STATUS_SUCCESS      0  
The function call was successfully executed.
```

```
#define EASI_STATUS_ERROR       -1  
The function call could not be executed due to a generic error.
```

```
#define EASI_STATUS_INVALID_PARAMETER -2  
An invalid parameter was passed to the function call.
```

```
#define EASI_STATUS_NOT_FOUND   -3  
In the current version of EASI this value has been reserved and therefore should not be used.
```

```
#define EASI_STATUS_READ_ERROR  -4  
A read error occurred while using the read functionality, for example during EasiI2CRead.
```

```
#define EASI_STATUS_WRITE_ERROR -5  
A write error occurred while using the write functionality, for example during EasiI2CWrite.
```

```
#define EASI_STATUS_TIMEOUT     -6  
Timeout error occurred.
```

## 5.2.3 Generic Board Information

The following function calls are to be used in order to obtain generic information about the Qseven™ module such as manufacturer name, serial number and product name.

```
unsigned long EasiBoardGetName(unsigned long dwID, char *pszName, unsigned long dwSize);  
unsigned long EasiBoardGetValue(unsigned long dwID, unsigned long *pdwValue);
```

```
// strings
```

```
#define EASI_BOARD_MANUFACTURER 0  
#define EASI_BOARD_NAME 1  
#define EASI_BOARD_SERIAL 2
```

```
// values
```

```
#define EASI_BOARD_BIOS_REVISION 3  
#define EASI_BOARD_BOOT_COUNTER 4  
#define EASI_BOARD_RUNNING_TIME_METER 5
```

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## 5.2.4 Storage Areas

The Qseven™ module may include a designated storage area to be used for customer specific data. This area, if present, offers at least 32bytes of persistent storage. A typical example of the use of this area would be for customer specific system serial numbers.

The read and write functions are used to read and write to the storage area and the size function is used to determine to exact size of the storage area. Currently only *dwID 0* is defined. Other values for *dwID* are intended for future use as enhancements of the API.

```
unsigned long EasiStorageAreaSize(unsigned long dwID);  
unsigned long EasiStorageAreaRead(unsigned long dwID, unsigned long dwOffset, unsigned char *pBytes,  
unsigned long dwLen);  
unsigned long EasiStorageAreaWrite(unsigned long dwID, unsigned long dwOffset, unsigned char *pBytes,  
unsigned long dwLen);
```

## 5.2.5 Watchdog

The EASI function for the Watchdog must be implemented in accordance to the following function description. The Watchdog has been specified as a single stage Watchdog that resets the system when timed out.

```
unsigned long EasiWDogTrigger(void);  
unsigned long EasiWDogSetConfig(unsigned long timeout, unsigned long delay, unsigned long mode);
```

## 5.2.6 I<sup>2</sup>C BUS

The EASI function for the I<sup>2</sup>C must be implemented in accordance to the following function description.

```
unsigned long EasiI2CRead(unsigned long dwID, unsigned char bAddr, unsigned char *pBytes, unsigned  
long dwLen);  
unsigned long EasiI2CWrite(unsigned long dwID, unsigned char bAddr, unsigned char *pBytes, unsigned  
long dwLen);  
unsigned long EasiI2CReadRegister(unsigned long dwID, unsigned char bAddr, unsigned short wReg,  
unsigned char *pDataByte);  
unsigned long EasiI2CWriteRegister(unsigned long dwID, unsigned char bAddr, unsigned short wReg,  
unsigned char bData);
```

For the above mentioned function calls, *dwID* values are defined as follows in order to address different types of I<sup>2</sup>C Buses:

The primary I<sup>2</sup>C Bus is to be used for connecting external I<sup>2</sup>C devices such as temperature sensors while the LFP I<sup>2</sup>C Bus should be used for display detection.

```
#define EASI_I2C_PRIMARY 0  
#define EASI_I2C_LFP 1
```

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## 5.2.7 LCD Control

The EASI function for the LCD Control must be implemented in reference to the following function description.

These calls are used to increase or decrease the backlight intensity. They utilize a value from 0 to 100 whereby 0 represents backlight off and 100 equals full intensity.

```
unsigned long EasiVgaGetBacklight(unsigned long *pdwSetting);  
unsigned long EasiVgaSetBacklight(unsigned long dwSetting);
```

## 5.2.8 Temperature Control

This function is used to obtain the temperature value of the Qseven™ module and is provided in units of 1 degree centigrade. Currently, only *dwID 0* is defined and specifies CPU temperature. Other values for *dwID* are intended for future use as enhancements of the API.

```
unsigned long EasiTemperatureGetCurrent(unsigned long dwID, unsigned long *pdwSetting);
```

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## 6 Industry Specifications

The list below provides links to industry specifications used to define the Qseven™ interface specification.

**Table 6-1 Industry Specifications**

Specification	Description	Link
1000BASE T	IEEE standard 802.3ab 1000BASE T Ethernet	<a href="http://www.ieee.org/portal/site">www.ieee.org/portal/site</a>
ACPI	Advanced Configuration and Power Interface Specification Rev. 3.0a	<a href="http://www.acpi.info">www.acpi.info</a>
DisplayID	Display Identification Data (DisplayID) Structure, Version 1.0	<a href="http://www.vesa.org">www.vesa.org</a>
DisplayPort	DisplayPort Standard - Version 1.1a	<a href="http://www.vesa.org">www.vesa.org</a>
DVI	Digital Visual Interface, Rev 1.0, April 2, 1999, Digital Display Working Group	<a href="http://www.ddwg.org">www.ddwg.org</a>
ExpressCard	ExpressCard Standard Release 1.0	<a href="http://www.expresscard.org">www.expresscard.org</a>
HDA	High Definition Audio Specification, Rev. 1.0	<a href="http://www.intel.com/standards/hdaudio">www.intel.com/standards/hdaudio</a>
I2C	The I2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1	<a href="http://www.semiconductors.philips.com">www.semiconductors.philips.com</a>
IEEE 802.3-2002	IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications	<a href="http://www.ieee.org">www.ieee.org</a>
LPC	Low Pin Count Interface Specification, Revision 1.0 (LPC)	<a href="http://developer.intel.com/design/chipsets/industry/lpc.htm">developer.intel.com/design/chipsets/industry/lpc.htm</a>
LVDS	Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor	<a href="http://www.national.com">www.national.com</a>
LVDS	LVDS Owner's Manual	<a href="http://www.national.com">www.national.com</a>
LVDS	ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001.	<a href="http://www.ansi.org">www.ansi.org</a>
PCI Express	PCI Express Base Specification, Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved	<a href="http://www.pcisig.com">www.pcisig.com</a>
PCI Express	PCI Express Base Specification, Revision 1.1 PCI Express Card Electromechanical Specification, Revision 1.1	<a href="http://www.pcisig.com/specifications">www.pcisig.com/specifications</a>
SATA	Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved	<a href="http://www.sata-io.org">www.sata-io.org</a>
SATA	Serial ATA Specification, Revision 1.0a	<a href="http://www.serialata.org">www.serialata.org</a>
SDVO	SDVO (Serial Digital Video Out) is a proprietary Intel technology introduced with their 9xx-series of chipsets.	<a href="http://en.wikipedia.org/wiki/SDVO">en.wikipedia.org/wiki/SDVO</a>
Smart Battery	Smart Battery Data Specification, Revision 1.1, December 11, 1998	<a href="http://www.sbs-forum.org">www.sbs-forum.org</a>
SMBUS	System Management Bus (SMBUS) Specification,	<a href="http://www.smbus.org">www.smbus.org</a>

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USB	Universal Serial Bus (USB) Specification, Revision 2.0	<a href="http://www.usb.org/home">www.usb.org/home</a>